In the Claims:

Claim 1 (previously presented): A process for fabricating a semiconductor device comprising the steps of:

providing a semiconductor substrate;

forming a silicon nitride layer overlying the substrate;

deposition a layer of polycrystalline silicon overlying the silicon nitride layer;

forming an anti-reflective coating overlying the layer of polycrystalline silicon, the anti-reflective coating comprising a first layer of oxide and a second layer of silicon oxynitride overlying the first layer;

pattern etching the anti-reflective coating, the layer of polycrystalline silicon and the silicon nitride layer to form a stack, the stack having an edge and a top;

removing the remaining layer of silicon oxynitride in the stack by etching in hot phosphoric acid before subjecting the layer of silicon oxynitride to any temperature greater than about 400°C;

oxidizing the layer of polycrystalline silicon in the stack after the step of removing the remaining layer of silicon oxynitride in the stack.

Claims 2-5 (canceled).

2 **Claim 6 (original):** The process of claim 1 wherein the step of forming an anti-reflective coating comprises the step of depositing a thin layer of silicon oxide by chemical vapor deposition from a TEOS source.

3 **Claim 7 (original):** The process of claim 1 wherein the step of forming an anti-reflective coating comprises the step of depositing a layer of silicon oxynitride by plasma enhanced chemical vapor deposition from reactants N_2O and SiH_4.

4 **Claim 8 (original):** The process of claim 7 wherein the ratio of SiH_4 to N_2O reactants is maintained at about 1.22:1.

5 **Claim 9 (original):** The process of claim 7 wherein the ratio of SiH_4 to N_2O reactants is maintained in the range of about 0.9-1.5:1.

6 **Claim 10 (previously presented):** A process for etching silicon oxynitride which comprises the steps of:

depositing a layer of polycrystalline silicon overlying a substrate;

depositing a layer of silicon oxynitride overlying the layer of polycrystalline silicon;

pattern etching the layer of silicon oxynitride and the layer of polycrystalline silicon to form a stack, the stack having an edge: and

etching the remaining layer of silicon oxynitride in the stack in a phosphoric acid etchant without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride;

forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack.

Claims 11-13 (canceled).

Claim 14 (previously presented): A process for fabricating a semiconductor device comprising the steps of:

depositing a layer of polycrystalline silicon overlying a substrate;

depositing a first layer of oxide to a thickness of between about 7.5nm and 10nm by chemical vapor deposition from a TEOS source overlying the layer of polycrystalline silicon;

depositing a second layer of silicon oxynitride overlying the first layer to a thickness of between about 25nm and about 30nm by plasma enhanced chemical vapor deposition;

pattern etching the first and second layers and the layer of polycrystalline silicon to form a stack; and

etching the second layer in the stack in an etchant comprising hot phosphoric acid, the etching occurring before the second layer is subjected to any temperature greater than about 400°C;

oxidizing the layer of polycrystalline silicon in the stack after the step of etching the second layer in the stack.

8 **Claim 15 (original):** The process of claim 14 wherein the step of depositing a second layer of silicon oxynitride comprises depositing a layer from reactants comprising N_2O and SiH_4 and controlling the ratio of reactants to vary the extinction coefficient of the second layer.

9 **Claim 16 (original):** The process of claim 15 wherein the ratio of reactants (SiH_4 to N_2O) is controlled to about 0.9-1.5:1.

10 **Claim 17 (original):** The process of claim 16 wherein the ratio of reactants is controlled to about 1.22:1.

11 **Claim 18 (previously presented):** A process comprising:

providing a semiconductor substrate;

forming a gate oxide above the semiconductor substrate;

forming a first polycrystalline silicon layer over the gate oxide;

forming an interpoly dielectric;

forming a second polycrystalline silicon layer over the interpoly dielectric;

depositing a layer of silicon oxynitride above the second polycrystalline silicon layer;

pattern etching the layer of silicon oxynitride, the second polycrystalline silicon layer, the interpoly dielectric, the first polycrystalline silicon layer, and the gate oxide to form a stack, the stack having an edge; and

removing the layer of silicon oxynitride in the stack without subjecting the layer of silicon oxynitride to a temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride;

forming a layer of oxide on the edge of the stack after the step of removing the layer of silicon oxynitride in the stack.

Claim 19 (canceled).

12 **Claim 20 (previously presented):** The process of claim 18, wherein the layer of silicon oxynitride is deposited by a plasma enhanced chemical vapor deposition process using the reactants N_2O and SiH_4.

13 **Claim 21 (previously presented):** The process of claim 20, wherein the ratio of SiH_4 to N_2O is maintained in the range of about 0.9-1.5:1.

14 **Claim 22 (previously presented):** The process of claim 20, wherein the ratio of SiH_4 to N_2O is maintained at about 1.22:1.

15 **Claim 23 (previously presented):** The process of claim 18, wherein the interpoly dielectric is silicon nitride.

16 **Claim 24 (previously presented):** The process of claim 18, wherein the removing of the layer of silicon oxynitride comprises the step of etching with hot phosphoric acid.

Claim 25 (canceled).

17 **Claim 26 (previously presented):** A process comprising:

depositing a layer of polycrystalline silicon over a substrate;

depositing a layer of silicon oxynitride above the layer of polycrystalline silicon;

pattern etching the layer of silicon oxynitride and the layer of polycrystalline silicon to form a stack, the stack having an edge;

removing the layer of silicon oxynitride in the stack before subjecting the layer of silicon oxynitride to a temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride, and

forming a layer of oxide on the edge of the stack after the step of removing the layer of silicon oxynitride in the stack.

Claim 27 (canceled).

18 **Claim 28 (previously presented):** The process of claim 26, wherein the layer of silicon oxynitride is deposited by a plasma enhanced chemical vapor deposition process using the reactants N_2O and SiH_4.

19 **Claim 29 (previously presented):** The process of claim 28, wherein the ratio of SiH_4 to N_2O is maintained in the range of about 0.9-1.5:1.

20 **Claim 30 (previously presented):** The process of claim 29, wherein the ratio of SiH_4 to N_2O is maintained at about 1.22:1.

21 **Claim 31 (previously presented):** The process of claim 26, wherein the removing of the layer of silicon oxynitride comprises the step of etching with hot phosphoric acid.

Claims 32-36 (canceled).